Chapter 6
Programmable Logic and Software
Programmable Logic and Software

- SPLD, CPLD, FPGA, PAL, GAL are all types of integrated circuits that are configurable through software.
- They were conceived to solve problems of cost and reliability created as the complexity of logic systems grew.
- They are all variations on a theme: make a general purpose IC that can be configured through programming to be used for specific logic designs.
- There is a need for 2 types of programmable device:
  - One-time programmable = cheapest implementation used for production.
  - Reprogrammable = can be upgraded by reinstalling the programming.
    - Reprogrammable devices can be either volatile or non-volatile depending on the technology used to implement them.
Programmable Logic Devices

- **FPGA Manufacturers:**
  - Actel, Altera, Aeroflex UTMC, Atmel, Lattice Semiconductor, NEC, QuickLogic, Xilinx

- **PLD & PAL Manufacturers:**
  - Altera, Atmel, Cypress Products, Lattice Semiconductor, Texas Instruments Xilinx

- **ASIC Manufacturers:**

- **IP Core Manufacturers:**
  - 4i2i Communications, Agere Systems, Amphion, Arc, Axeon, Bluewater Systems, Cast, CG-CoreEL programmable Solutions, CommStack, DCM Technologies .... and on and on .....
Programmable Logic: SPLDs and CPLDs

- SPLD: The PAL (Programmable Array Logic)
  - Implementing a Sum-of-Products Expression

SPLD = Simple Programmable Logic Device
CPLD = Complex Programmable Logic Device
Programmable Logic: SPLDs and CPLDs

- SPLD: The GAL (reprogrammable PAL)

GAL = Generic Array Logic
SPLD = Simple Programmable Logic Device

The fuses have been replaced with an EEPROM style link.
Programmable Logic: SPLDs and CPLDs

- Simplified Notation for PAL/GAL Diagrams

Uses notation to simplify drawing
Programmable Logic: SPLDs and CPLDs

- PAL/GAL General Block Diagram

Note that we can combine any of the inputs to form SOP expressions at the outputs.
Programmable Logic: SPLDs and CPLDs

- Macrocells

(a) Combinational output (active-LOW). An active-HIGH output would be shown without the bubble on the tristate gate symbol.

(b) Combinational input/output (active-LOW)

(c) Programmable polarity output
Programmable Logic: SPLDs and CPLDs

- Specific SPLDs
  - In applying programmable logic devices we have to select the device to fit the application.
  - Determine the number of input variable needed
  - Determine the number of outputs that need to be specified
  - The logic gate density to make sure there is enough logic to implement our design
  - Operating frequency
  - Propagation delay times
  - DC supply voltage
Programmable Logic: SPLDs and CPLDs

- The CPLD
  - Multiple SPLD arrays with programmable interconnections
  - Organizes the SPLD arrays into LABs (logic array blocks)
  - The network that interconnects the LABs is the PIA (programmable interconnect array)
  - CPLDs are made in “families” - a collection of similar devices that range in density and I/O capability.
  - Different manufacturers implement this scheme differently but all are similar in their intent.
Altera CPLDs

- **MAX 7000 CPLD**
  - A family of CPLD manufactured by Altera
  - It is a classic PAL/GAL structure that produces SOP functions.
  - Different members of the family have differing numbers of LABs and differing number of interconnect pins.
Altera CPLDs

- Max 7000 Versatility
  - Has Shared and Parallel Expanders to increase versatility:
    - Shared = input sharing, Parallel = output sharing
Altera CPLDs

- The MAX II CPLD
  - A different implementation using a Lookup Table (LUT) to implement the AND/OR array.
  - It also has a different row and column organization

(a) Look-up table logic. A 1 is stored at each product term address.
(b) AND/OR array logic
Xilinx CPLDs

- PLA (Programmable Logic Array)
  - Basic organization of the Xilinx CoolRunner II family of CPLDs
  - PLA vs PAL comparison:

Note that the PLA has 4 SOP outputs vs 1 for the PAL
Xilinx CPLDs

- Cool Runner II
  - Uses the PLA architecture
  - Multiple function blocks (similar to LABs)
  - Uses an “Advanced Interconnect Matrix” (AIM)
Programmable Logic: FPGAs

- **Introduction**
  - Uses different architecture than CPLDs (does not use PAL/GAL or PLA type logic blocks)
  - Much greater density than CPLDs
  - More equivalent gates than a CPLD
  - Smaller logic producing elements but a lot more of them
  - The PIA (programmable interconnects) are arranged in rows and columns.
Programmable Logic: FPGAs

- Configurable Logic Blocks
  - Somewhat analogous to macrocells.
  - Basic building units of a FPGA
  - Each CLB is made up of multiple smaller logic modules and local programmable interconnects.

Logic Modules can be configured as combinational logic, registered logic, or a combination of both. A flip-flop is part of the logic and is used for registered logic.
SRAM-Based FPGAs

- FPGAs can be either volatile or nonvolatile.
- Volatile FPGAs use SRAM technology.
  - All programmed data is lost when power is removed
  - To get around this, many contain either nonvolatile memory embedded on the chip or download the program from a host processor each time it is powered up.

Programmable Logic: FPGAs
FPGA Cores

- FPGAs can contain pre-programmed “modules” that perform specific functions (embedded processors, registers, digital signal processors, etc)
- These functions can be implemented in two ways:
  - Hard Core: a portion of the FPGA is manufactured with the function.
  - Soft Core: the FPGA can be programmed with this function
Altera FPGAs

- Altera is another manufacturer of FPGAs
  - Architecture is based upon use of LUT structures and generic FPGA organization.
- The Logic Array Block (LAB)

Each ALM can be programmed for two combinational logic outputs or registered outputs. It also has adder logic, flip-flops and other logic for arithmetic, counter and shift register functions.
Altera FPGAs

- The Adaptive Logic Module (ALM)
  - The ALM has 4 operating modes:
    - Normal mode – used primarily for generating combinational logic functions. Can produce two SOP functions with a combination of input variables
    - Extended LUT mode – allows expansion to 7 input variables
    - Arithmetic mode
    - Shared Arithmetic mode

Normal Mode

Extended LUT Mode
Altera FPGAs

• Embedded Functions
  - Embedded functions such as memory, digital signal processors, and more I/O blocks can be built into these FPGAs
Xilinx FPGAs

- Xilinx is another manufacturer of FPGAs
  - Of the several different families produced by Xilinx, most use traditional FPGA architecture
  - But there are some that are moving into the application specific oriented areas

- Configurable Logic Blocks
  - Consists of Logic Cells, Slices
  - A 4-input LUT can make
    - One product term
    - Or an SOP with up to 16 product terms
Xilinx FPGAs

- **SOP Cascade Chains**
  - Provides for the interconnect of slices to create more complex SOP expressions
    - Slices can be used alone or cascaded
    - The MUX provides for the cascading
    - 1 slice = 8-input, 1 product term
    - 2 slices = 16-input, 2 product terms
    - 4 slices = 32-input, 4 product terms
    - More expansion by using more CLBs
Xilinx FPGAs

- Traditional FPGA Architecture vs. ASMBL Architecture
  - ASMBL (Application Specific Modular Block)
  - Uses columnar structure rather than row/column architecture
  - I/O is interspersed throughout the chip rather than around the perimeter.
  - Each column can be an embedded function such as configurable logic blocks, I/O blocks, memory, or hard or soft IP cores such as digital signal processors.
  - These logic strips (columns) can be intermixed to meet specific application requirements.
Programmable Logic Software

• Introduction
  - Since these devices are programmable, there must be tools to program them.
  - Each manufacturer offers tools to do the programming, some are free, others cost a considerable amount of money.
  - These programming suites also offer design and verification assistance to the designer to help debug the design before the device is programmed.
  - Many also contain revision control facilities to help with manufacturing releases of different versions of the application.

We have been using this type of software for most of our lab exercises.
Programmable Logic Software

- Design Entry
  - Designs can be entered into the software in two ways
    - VHDL or some other language – uses text entry and is basically a programming language
    - Schematic entry – a graphical method of entering the design using standard logic symbols
Programmable Logic Software

• Functional Simulation
  - The programmed logic functions can be simulated in the software
  - Examination of the simulation helps insure that each state is correct in the application.
  - The simulation is completed before the application is downloaded into the chip.

Each output state can be compared to the inputs to verify proper operation.
Programmable Logic Software

- Synthesis
  - Prepares the design for downloading onto the target device
  - Optimizes the design to conserve logic gates and other resources
  - Creates the “Netlist”
    - A connectivity list that describes how the components are interconnected
    - Defines all of the input and output pins and how they are connected to the internal gate structures
    - Creates the “wires” connecting all of the internals
  - The Netlist is used by the compiler to define how the chip is programmed.
Programmable Logic Software

- Implementation (Software)
  - The implementation phase of the process uses the netlist to generate the instructions to program a specific device.
  - The software has profiles for many (or all) of the devices by that manufacturer
  - When implementing the program, these profiles are used to provide specific routing information for programming
Programmable Logic Software

- **Timing Simulation**
  - Timing simulation is performed prior to downloading
  - It checks for any glitches or problems with propagation delays in the circuit.
Programmable Logic Software

- Device Programming (Downloading)
  - After the program has been verified, simulated, and compiled, it is downloaded into the target device.
  - The development program usually has the capability of communicating with the device and programming it
  - However, some manufacturers make programmers to burn the chips