Chapter 9
Latches, Flip-Flops, and Timers
Latches

- A temporary storage device that has two stable states (bistable)
- The S-R (Set-Reset) Latch (also called a multivibrator)

When Q is HIGH, \( \bar{Q} \) is LOW, and when Q is LOW, \( \bar{Q} \) is high

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>R</td>
<td>Q</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
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<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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</tbody>
</table>

Truth Table for an Active-Low Input S-R latch.
Latches

- An Application – Switch Debouncing

Switch contacts bounce when they make, creating several on/off signals that the logic will interpret as several switch closures. The latch will change state on the first transition and remain there until reset.
Latches

- The 74LS279 Set-Reset Latch

This is a quad package. Note that each latch has two active low set inputs and an active high output.
Latches

• The Gated S-R Latch
  - Includes an Enable line
  - The output state changes only when the enable line is brought high

![Logic diagram and logic symbol](image.png)

Note the pulses on the EN line that change the state of Q depending on the S or R input state.
Latches

- The Gated D Latch
  - D Latches are simpler circuits than the S-R latch
  - The Output (Q) follows the input only when the Enable line is high.

Note that the output only follows the input when the enable is High.
Latches

- The 74LS75 D Latch

This is a quad D Latch package with 4 Latches but only 2 Enable lines.
Edge-Triggered Flip-Flops

- Flip-flops are synchronous bistable devices known as bistable multivibrators
- They are edge triggered to insure a known transition point (although there have been some level triggered devices in the past)
- Their inputs change on a control input called the clock (CLK)
- All changes occur in sync with the clock input
Edge-Triggered Flip-Flops

- Edge-triggered flip-flop

Three styles of flip-flops: S-R, D, and J-K all of which are edge-triggered (note the > on the C input).
- The top row is positive edge triggered.
- The bottom row is negative edge triggered.
The Edge-Triggered S-R Flip-Flop

- The Edge-Triggered S-R Flip-Flop

Note that this is a positive edge triggered device.

The S-R flip-flop is not available in IC form.
A Method of Edge-Triggering

Edge-Triggered Flip-Flops

- A Method of Edge-Triggering

The NAND gates insure that the S and R inputs only reach the latch when the CLK pulse goes high.

The Pulse transition Detector, looks for the rising edge of the CLK input.
Edge-Triggered Flip-Flops

- The Edge-Triggered D Flip-Flop

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<th>Comments</th>
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<tbody>
<tr>
<td>D</td>
<td>CLK</td>
<td>Q</td>
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<td>↑</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>↑</td>
<td>0</td>
</tr>
</tbody>
</table>

Pinout

Functional Diagram
Edge-Triggered Flip-Flops

- The Edge-Triggered J-K Flip-Flop
  - The J-K flip-flop has no invalid state (the S-R does)

If both J and K are HIGH the output will toggle on each successive rising clock edge.
Edge-Triggered Flip-Flops

- Asynchronous Preset and Clear Inputs
  - Provide for either clearing the output or presetting them independent of the clock.
  - Generally they are labeled Preset (PRE) and Clear (CLR) but some manufacturers call them Set and Reset.
  - Usually they are active low.

74LS76 Functional Diagram
Flip-Flop Operating Characteristics

- **Propagation Delay Times**
  - The interval of time required after an input signal has been applied for the resulting output change to occur.
  - Different signals take different paths through the gate electronics.
  - Four categories of propagation delay:
    - A) Propagation delay for low to high transition of the output.
    - B) Propagation delay for high to low transition of the output.
    - C) Propagation delay measured from leading edge of preset to low to high transition of the output.
    - D) Propagation delay measured from the leading edge of the clear input to the high to low transition of the output.
Flip-Flop Operating Characteristics

• Set-up Time
  - The minimum amount of time required for the logic levels to be maintained constantly on the inputs (J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliable clocked into the flip-flop.

The signal, D, must appear on the pin at least $t_s$ seconds before the rising edge of the clock in order to insure reliable data.
Flip-Flop Operating Characteristics

• Hold Time
  - The minimum amount of time required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop.

The hold time is necessary to give the flip-flop time to stabilize from the clock transition.
Flip-Flop Operating Characteristics

- **Maximum Clock Frequency** ($f_{\text{max}}$)
  - The highest rate the flip-flop can be triggered.
- **Pulse Widths** ($t_w$)
  - Minimum pulse widths for reliable operation for the clock, preset, and clear inputs.
- **Power Dissipation** ($P_d$)
  - The total power consumption of the device
  - e.g. For a 5 ma gate: $P = V_{cc} \times I_{cc} = 5\text{v} \times 5\text{ma} = 25\text{mw}$
Flip-Flop Applications

- Parallel Data Storage

This is a basic register architecture used in many digital applications.
Flip-Flop Applications

- Frequency Division

Some parts of digital systems operate at a slower rate than the clock. (Serial I/O, A/D conversion, etc.) Flip-flops can be used to divide the master clock frequency into slower clock cycles for these applications. Note that the divided frequencies are still in sync with the master clock.

Cascading the flip-flops gives greater frequency division (divide by 2 for each section)
Flip-Flop Applications

• Counting
  - One of the most important applications of flip-flops is in digital counters.
  - Digital counters not only count things, but are useful as frequency meters, parts of A/D converters, etc.

Flip-flops can be cascaded to get a larger digital count from the device.
One-Shots

- A one-shot is a monostable multivibrator with only one stable state.
- It is used to create pulses because when it is triggered it moves to its unstable state, remains there for a predetermined amount of time then returns to its stable state.
- They are useful for creating “events” and triggering other devices.
- They are either retriggerable or nonretriggerable.
  - Nonretriggerable = will not respond to a trigger unless it has returned to its stable state.
  - Retriggerable = will lengthen the output pulse if triggered before returning to stable state.

The R-C series circuit provides a timing circuit to establish the pulse width.
One-Shots

- 74121 Nonretriggerable One-Shot

This device uses a Schmitt-Trigger that provides hysteresis to prevent erratic switching.
The 555 Timer

- An unusually versatile IC that can be configured for different modes of operation
  - Monostable multivibrator (one-shot)
  - Astable multivibrator (oscillator)

- Basic Operation
  - Comparator looks at external voltage
  - Discharge circuit can discharge a capacitor in a timing circuit
  - Threshold circuit used to set either mono or astable modes
The 555 Timer

- Monostable (One-Shot Operation)

A single pulse is output with a pulse width set by the timing circuit R1 and C1. C1 charges until it reaches the threshold when it triggers the beginning of the pulse. Q1 turns on and starts to discharge C1 bringing it below the threshold resetting the timer.
The 555 Timer

• Astable Operation

Two different time constants are established by R1, R2 and C1. Note also that the Trigger input is connected to the Threshold input causing it to retrigger when C1 discharges.
CPLD Macrocells

- CPLD macrocells also contain flip-flops
- They can be configured for combinational logic (not using the flip-flops) or register logic (using the flip-flops)
- The Xilinx CoolRunner II Macrocell

This macrocell can be programmed to be either a combinational logic cell that generates SOP terms, or configured for registered logic functions that can use the flip flop to stage data and allow it to be clocked onto a data path.