• Conversion between analog and digital signals is common. The following aspects will be examined:
  – DAC and ADC
  – Troubleshooting
  – Different conversion methods
  – Analog multiplexing
  – DSP
11-1 Interfacing With the Analog World

• A review of the difference between digital and analog quantities
  – Digital quantities – values can take on one of two possible values. Actual values can be in a specified range so the exact value is not important.
  – Analog quantities – values can take on an infinite number of values, and the exact value is important.
11-1 Interfacing With the Analog World

- Transducer – converts physical variable to electrical variable
- ADC – analog to digital converter
- Computer – stores the digital value and does something with it
- DAC – Digital to analog converter
- Actuator – converts electrical variable to physical variable
11-2 Digital to Analog Conversion

• The conversion process:
  – Digital code is converted to a proportional voltage or current (see next page)
  – Reference voltage determines the max output DAC can output

• Analog (pseudo analog) output (output is in steps)

• Input weights (position in the binary number)
FIGURE 11-2 Four-bit DAC with voltage output.
Digital to Analog Conversion (continued)

• Resolution (step size)

\[ \text{resolution} = K = \frac{A_{fs}}{(2^n - 1)} \]

A five-bit D/A converter produces \( V_{out} = 0.2 \text{ V} \) for a digital input of 00001. Find the value of \( V_{out} \) for an input of 11111.

Solution:

0.2 V is the weight of the LSB. Thus, the weights of the other bits must be 0.4 V, 0.8 V, 1.6 V, and 3.2 V, respectively. For a digital input of 11111, the value of \( V_{out} \) will be \( 3.2 + 1.6 + 0.8 + 0.4 + 0.2 = 6.2 \text{ V} \)
A computer controls the speed of a motor. The 0 to 2 mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm. How many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed?

**Solution:**

The motor speed will range from 0 to 1000 rpm as the DAC goes from zero to full scale. Each step in the DAC output will produce a step in the motor speed. We want the step size to be no greater than 2 rpm. Thus, we need at least 500 steps (1000/2). Now we must determine how many bits are required. We know that the number of steps is $2^N - 1$ so: $2^N - 1 \geq 500 \Rightarrow 2^N \geq 501$. Since $2^8 = 256$ and $2^9 = 512$, the smallest number of bits must be 9.
11-2 Digital to Analog Conversion

- BCD input code converted to analog output

**Example: If** $A_0$ **is 0.1 V then:**

There are 99 steps (input is decimal)

Full Scale output = $99 \times 0.1 = 9.9$ V

Assume the input is: 0101 1000. What is $V_{out}$?

$V_{out} = C_1 + A_1 + D_0 = 4V + 1V + 0.8V = 5.8V$
Digital to Analog Conversion (continued)

• Bipolar DACs
  – Many DACs produce both positive and negative values
  – 2’s complement can be used to represent negative voltages

Example: Assume we have a six-bit bipolar DAC that uses 2’s the complement system and has a resolution of 0.2 V. The binary input values range from 100000 (-32) to 011111 (+31) to produce analog outputs in the range from -6.4 to +6.2 V. There are 63 steps ($2^6 - 1$) of 0.2 V between these negative and positive limits.
11-3 D/A Converter Circuitry

- A summing operational amplifier with a resolution of .625 V

**Example:** Determine a) the weight of each input bit, and b) change $R_f$ to 250 ohm and determine full-scale output.

**A)** The MSB passes with gain = 1, so its weight in the output is 5V. So:

- MSB = 5V, 2nd MSB = 5/2 = 2.5 V, 34th MSB = 5/4 = 1.25 V and 4th MSB = 5/8 = 0.625 V

**B)** $R_f$ is reduced by a factor of 4 => each input will be four times smaller than the above values.
Means to enhance Conversion Accuracy

Two things can cause inaccuracy: untrimmed resistors and varying input voltages from digital devices such as flip-flops.

The resistors are no problem.

The input voltage issue can be solved by using a precision reference supply.
Example: Assume that $V_{\text{REF}} = 10$ V and $R = 10k$ ohm. Determine the resolution and the full-scale output for this DAC. Assume that $R_L$ is much smaller than $R$.

Solution:

$I_{\text{out}} = V_{\text{REF}}/R = 1$ mA. This is the weight of the MSB. The other three currents will be 0.5, 0.25, and 0.125 mA. The LSB is 0.125 mA, which is also the resolution.

The full-scale output will occur when the binary inputs are all HIGH so that each current switch is closed and

$$I_{\text{out}} = 1 + 0.5 + 0.25 + 0.125 = 1.875$$ mA

Note that the output current is proportional to $V_{\text{REF}}$. If $V_{\text{REF}}$ is increased or decreased, the resolution and the full-scale output will change proportionally.
11-3 D/A Converter Circuitry

- R/2R ladder
  - Circuits with binary weighted resistors cause a problem due to the large difference in R values between LSB and MSB
  - The R/2R ladder uses resistances that span only a 2 to 1 range

Example: Assume that $V_{\text{REF}} = 5$ V. What is the resolution and full-scale output.

Solution:

The resolution is equal to the weight of the LSB, which we can determine by setting $B = 0001 = 1$ in equation (11-6):

$$\text{resolution} = \frac{-5V \times 1}{8} = -0.625V$$

The full-scale output occurs for $B = 1111 = 15_{10}$.

$$\text{full-scale} = \frac{-5V \times 15}{8} = -9.375V$$
11-4 DAC Specifications

• Many DACs are available as ICs or self contained packages. Key specifications are:
  – Resolution (in bits)
  – Accuracy (full-scale error, linearity error)
  – Offset error
  – Settling time
  – Monotonicity
    • Its output increases as the binary input is incremented from one value to the next.
    • The staircase output will have no downward steps as the binary input is incremented from zero to full scale.
11-5 An IC DAC

• AD7524
  – CMOS IC
  – 8 bit D/A
  – Uses R/2R ladder network
  – Max settling time is 100 ns
  – Full range accuracy is +/- 0.2% F.S.
  – Reference voltage can be negative and positive from 0 to 25 V
11-6 DAC Applications

- Used when a digital circuit output must provide an analog voltage or current
  - Control
    - Use a digital computer output to adjust motor speed or furnace temperature
  - Automatic testing
    - Computer generated signals to test analog circuitry
  - Signal reconstruction
    - Restoring an analog signal after it has been converted to digital. Audio CD systems, and audio/video recording
  - A/D conversion
  - Serial DACs
11-7 Troubleshooting DACs

- Logic probes/pulsers used for digital input
- Meter and oscilloscope used for analog output
- Static accuracy test
  - Binary input is set to a fixed value while analog output is checked with a very accurate meter
- Staircase test
  - Binary input is incremented and output is checked for problems on the “steps”
Example: How would the staircase waveform appear if the C input to the DAC is open? Assume that the DAC inputs are TTL-compatible.

Solution: An open connection at C will be interpreted as a constant logic 1 by the DAC. Thus, this will contribute a constant 4 V to the DAC output so that the DAC output will appear as shown below. The dotted lines are the staircase as it would appear if the DAC were working correctly. Note that the faulty output waveform matches the correct one during those times when the bit C input would normally be HIGH.
11-8 Analog to digital Conversion

- ADC – digital code represents the analog input
- Generally more complex and time consuming than DAC
- Several types of ADC use DAC circuits
- The Op amp comparator ADC
  - Variations differ in how the control section continually modifies numbers in the register
11-9 Digital Ramp ADC

- A binary counter is used as the register and allows clock to increment the counter a step at a time until $V_{AX}$.

1. A START pulse is applied to reset the counter to 0 and start a conversion.
2. With all 0s at its input, the DAC’s output will be $V_{AX} = 0V$.
3. Because $V_A > V_{AX}$, the comparator output, $EOC$, will be HIGH.
4. When START return LOW, the AND gate is enabled and clock pulses get through to the counter.
5. As the counter advances, the DAC output, $V_{AX}$, increases one step at a time.
6. This process continues until $V_{AX}$ reaches a step that exceeds $V_A$ by an amount equal to or greater than $V_T$. $EOC$ goes LOW and inhibits the flow of pulses into the counter.
**Example:** Assume the following values for the ADC: clock frequency = 1 MHz; \( V_T = 0.1 \text{ mV} \); DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values: a. The digital equivalent obtained for \( V_A = 3.728 \text{ V} \); b. The conversion time; c. The resolution of this converter

**Solution:**

a. The DAC has a 10-bit input and a 10.23 V F.S. output. Thus, the number of total possible steps is \( 2^{10} - 1 = 1023 \). The step size is 
\[
\frac{10.23V}{1023} = 10\text{ mV}
\]
This means that \( V_{AX} \) increases in steps of 10 mV as the counter counts up from 0. Because \( V_A = 3.728 \text{ V} \) and \( V_T = 0.1 \text{ mV} \), \( V_{AX} \) must reach 3.7281 V or more before the comparator switches LOW. This will require
\[
\frac{3.7281V}{10\text{ mV}} = 372.81 = 373 \text{ steps}
\]
At the end of the conversion, the counter will hold the binary equivalent of 373, which is 0101110101. This is the desired digital equivalent of \( V_A = 3.728 \text{ V} \).

b. Three hundred seventy three steps were required to complete the conversion. Thus, 373 clock pulses occurred at the rate of one per microsecond. This gives a total conversion time of 373 \( \text{us} \).

c. The resolution of this converter is equal to the step size of the DAC, which is 10 mV. Expressed as a percentage it is \( 1/1023 \times 100\% = 0.1\% \).
11-9 Digital Ramp ADC

- A/D resolution and accuracy
  - Measurement error is unavoidable
  - Reducing the step size can reduce but not eliminate potential error
  - This is called quantization error
- Conversion time is illustrated at right:

Maximum conversion time will occur when VA is just below full scale so that VAX must go to the last step to activate EOC. For an N-bit converter this will be: $t_c(\text{max}) = (2^N - 1)$ clock cycles.

For this DAC, the maximum conversion time:

$$t_c(\text{max}) = (2^{10} - 1) \times 1 \text{ us} = 1023 \text{ us}$$
11-10 Data Acquisition

- Applications require analysis or storage of continuous waveform data.
- We “sample” the data at discrete points.
- The uComputer issues sampling requests to an ADC which converts the data and sends it to the uComputer.
11-10 Data Acquisition

- Digitizing analog data and transferring to memory is data acquisition
- Acquiring a single data point value is sampling
- Reconstructing a digitized signal:

<table>
<thead>
<tr>
<th>Point</th>
<th>Actual Voltage</th>
<th>Digital Equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>1.22</td>
<td>01111010</td>
</tr>
<tr>
<td>b</td>
<td>1.47</td>
<td>10010011</td>
</tr>
<tr>
<td>c</td>
<td>1.74</td>
<td>10101110</td>
</tr>
<tr>
<td>d</td>
<td>1.70</td>
<td>10101010</td>
</tr>
<tr>
<td>e</td>
<td>1.35</td>
<td>10000111</td>
</tr>
<tr>
<td>f</td>
<td>1.12</td>
<td>01110000</td>
</tr>
<tr>
<td>g</td>
<td>0.91</td>
<td>01011011</td>
</tr>
<tr>
<td>h</td>
<td>0.82</td>
<td>01010010</td>
</tr>
</tbody>
</table>
11-10 Data Acquisition

• Aliasing
  – Caused by under sampling
  – Harry Nyquist
    • The sampling frequency must be at least twice the highest input frequency
    • Sampling at a frequency less than twice the input frequency results in under sampling and incorrect reproduction

Frequency = 1.9 kHz
500usec sample rate
($F_s = 2$ kHz)

Aliased waveform = cosine at 100 Hz
Note that the alias frequency is the difference between the signal frequency and the sampling frequency.
11-11 Successive Approximation ADC

- Widely used ADC
- More complex than digital ramp but has a shorter conversion time
- Conversion time is fixed and not dependent on the analog input
- Many SACs are available as ICs.
Example: Choose a four-bit converter with a step size of 1 V. The four register bits feeding the DAC have weights of 8, 4, 2, and 1 V.

Assume the the analog input is \( V_A = 10.4 \) V. The operation begins with the control logic clearing all of the register bits to 0 = \([Q] = 0000\). The DAC output \( V_{AX} = 0 \) V. as indicated at time \( t_0 \) on the timing diagram. With \( V_{AX} < V_A \), the comparator output is HIGH.

At the next time step (\( t_1 \)) the control logic sets the MSB of the register to 1 so that \([Q] = 1000\). This produces \( V_{AX} = 8 \) V. Because \( V_{AX} < V_A \) the COMP output is still high. This HIGH output tells the control logic that the setting of the MSB did not make \( V_{AX} \) exceed \( V_A \), so that the MSB is kept at 1.

The Control logic now proceeds to the next lower bit, \( Q_2 \). It sets \( Q_2 \) to 1 to produce \([Q] = 1100\) and \( V_{AX} = 12 \) V at time \( t_2 \). Because \( V_{AX} > V_A \), the COMP output goes LOW. This LOW signals the control logic that the value of \( V_{AX} \) is too large, and the control logic then clears \( Q_2 \) back to 0 at \( t_3 \). Thus, at \( t_3 \), the register contents are back to 000 and \( V_{AX} \) is back to 8 V.

The next step occurs at \( t_4 \), where the control logic sets the next lower bit \( Q_1 \) so that \([Q] = 1010\) and \( V_{AX} = 11 \) V. With \( V_{AX} < V_A \), COMP is HIGH and tells the control logic to keep \( Q_1 \) set at 1.

The final step occurs at \( t_5 \), where the control logic sets the next lower bit \( Q_0 \) so that \([Q] = 1011\) and \( V_{AX} = 11 \) V. Because \( V_{AX} > V_A \), COMP goes LOW to signal that \( V_{AX} \) is too large, and the control logic clears \( Q_0 \) back to 0 at \( t_6 \).
Example: An eight-bit SAC has a resolution of 20 mB. What will its digital output be for an analog input of 2.17 V?

Solution: \[
\frac{2.17 \text{ mV}}{20 \text{ mV}} = 108.5
\]

So that step 108 would produce \( V_{AX} = 2.16 \text{ V} \) and step 109 would produce 2.18 V. The SAC always produces a final \( V_{AX} \) that is at the step below \( V_A \). Therefore, for the case of \( V_A = 2.17 \text{ V} \), the digital result would be \( 108_{10} = 01101100_2 \)

Conversion Time: The control logic goes to each register bit sets it to 1, decides whether or not to keep it at 1, and goes on the next bit. The processing of each bit takes one clock cycle, so that the total conversion time for an N-bit SAC will be N clock cycles. That is:

\[
t_c \text{ for SAC} = N \times 1 \text{ clock cycle}
\]

This conversion time will be the same regardless of the value of \( V_A \) because the control logic must process each bit to see whether or not a 1 is needed.
11-11 Successive Approximation ADC

• The ADC0804 – 20 pin CMOS IC

• Has 2 analog inputs (differential inputs). Can be connected as either single-ended or differential.

• Converts analog to eight-bit digital output.

• Has tri-state buffered outputs so that they can be connected in a data bus arrangement.

• With 8-bits, the resolution is 5 V/255 = 19.6 mV

• Has an internal clock with \( f = 1/(1.1RC) \), where \( R \) and \( C \) are external components. Typical frequency is 606 kHz for \( R = 10 \text{ kohm} \) and \( c = 150 \text{ pF} \). An external clock can be used if desired.

• At 606 kHz conversion time is approx. 100 us.

• Separate analog and digital grounds.
11-12 Flash ADCs

- High speed conversion
- Much more complex circuitry
  - 6 bit flash ADC requires 63 analog comparators
  - 8 bit flash ADC requires 255 comparators
  - 10 bit flash ADC requires 1023 comparators
- A 3 bit flash converter is shown at right
- Conversion time – No clock signal is used, so the conversion is continuous. This makes for very short conversion times, typically under 17 ns.
There are many other methods of A/D conversion. Each has pros and cons:

- Up/down digital-ramp ADC (tracking ADC)
  - Does not reset for each conversion
- Dual slope integrating ADC
  - Slow but cheap
  - Relatively insensitive to noise and component variations from temperature changes
- Voltage to frequency ADC
  - Converts to a frequency that is then digitized using a counter
  - Difficult to achieve accuracies better than 0.1%
- Sigma/delta modulation
  - Does not produce a multibit number but rather varying density of 1’s and 0’s
  - The pattern of the output data stream determines the average analog output

The method used will depend on the application
11-14 Digital Voltmeter

- Converts an analog voltage to BCD, decodes, and displays the value.
- Example:
  - Digital ramp ADC
  - 3 cascaded BCD counters (step size of 10 mV)
  - Full scale output of 9.99 V
  - Each BCD counter drives 4 bit register
  - Register feeds a decoder/driver and display
**Example:** Assume that $V_A$ is 6.372 V. In order for the COMP output to switch LOW, $V_A$ must exceed 6.3721 V. Because the DAC output increases by 10 mV/step, this requires:

$$\frac{6.3721V}{10 \text{ mV}} = 637.21 \rightarrow 638 \text{ steps}$$
11-14 Digital Voltmeter

• Several ranges can be read using attenuators and amplifiers

• Current and resistance can also be measured by modifying the circuit
  – Current is measured by passing the unknown current through a reference resistance and measuring the voltage
  – Resistance is measured by passing a reference current through an unknown resistance and measuring the voltage
11-15 Sample and Hold Circuits

- Solves problems caused by analog voltage changes during conversion time
- The significance of acquisition time: the capacitor ($C_h$) needs time to fully charge. The amount of time the switch needs to be closed is called the “acquisition time.”

*Control = 1 → switch closed → sample mode
*Control = 0 → switch open → hold mode
11-16 Multiplexing

- Multiple analog signals can be converted through time sharing of an ADC
- The process is illustrated in figure 11-27
  - The multiplexing clock controls the rate at which the analog signals are switched to the ADC
  - CMOS semiconductor switches can be used to reduce switch delay time
- The ADC0808 can multiplex eight different analog inputs to one ADC
FIGURE 11-27 Conversion of four analog inputs by multiplexing through one ADC.

Operation:

1. With select address = 00, VA0 is connected to the ADC input.
2. The control circuit generates a START pulse to initiate conversion.
3. When complete, EOC signals that the ADC output data are ready.
4. The multiplexing clock increments the select address to 01, which connects VA1 to the ADC.
5. Steps 2 and 3 are repeated.
6. The multiplexing clock increments the select address to 10 connecting VA2 to the DAC.
7. Steps 2 and 3 are repeated.
8. The multiplexing clock increments the select address to 11, and VA3 is connected to the ADC.
9. Steps 2 and 3 are repeated.
11-17 Digital Storage Oscilloscope

- Makes use of D/A and A/D converters
- Advantages of the DSO over the CSO
  - Waveform storage
  - Stored waveform display for comparison
  - Store and display waveforms before the trigger point
  - Print waveforms or transfer to a PC
11-17 Digital Storage Oscilloscope

- Figure 11-28 below is a block diagram of a DSC
11-18 Digital Signal Processing

- Specialized microprocessor optimized for repetitive calculations on streams of digitized data
- DSP is used frequently in filtering and conditioning of analog signals
  - Perform the same function as analog filters but allow greater flexibility
  - Can perform dynamic frequency adjustment
11-18 Digital Signal Processing

• Digital filtering process
  – Read the newest sample from A/D
  – Replace the oldest sample with the new one
  – Multiply each of the 256 samples by corresponding weight constant
  – Add all products
  – Output the resulting sum of products to the D/A
11-18 Digital Signal Processing

• Figure 11-30 shows the basic architecture of a DSP
11-18 Digital Signal Processing

- DSP concepts involve: ADC and DAC, data acquisition, sampling, signed binary numbers, signed binary addition and multiplication, and shift registers
- DSP applications:
  - Filters in CD players to minimize quantization noise
  - Echo canceling in telephone systems
  - PC modems
  - Musical instrument special effects
  - Digital television
  - Voice recognition
- DSP continues to grow into almost all electronic systems